High Performance Multibit Σ-Δ DAC with SACD Playback

AD1955

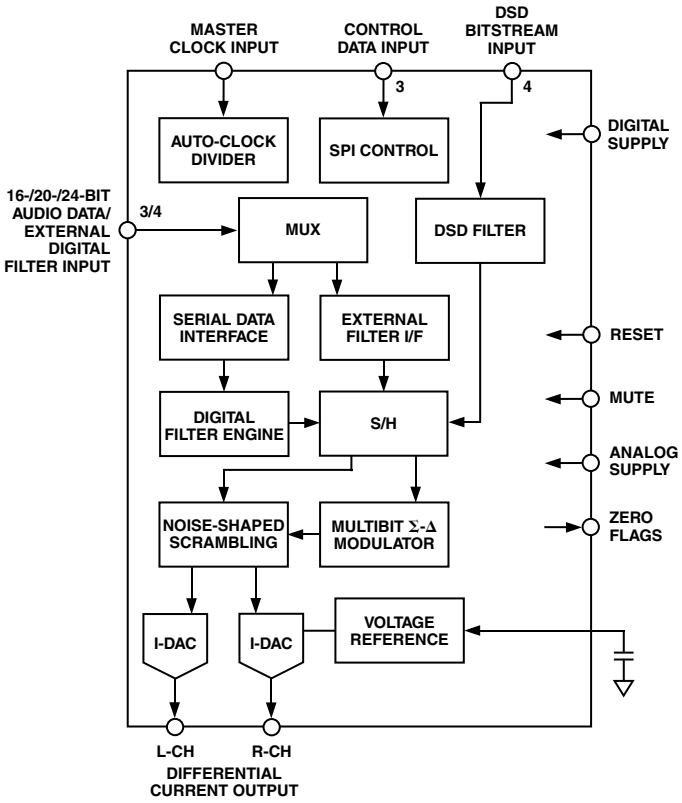
FEATURES

5 V Power Supply Stereo Audio DAC System
Accepts 16-/18-/20-/24-Bit Data
Supports 24-Bit, 192 kHz Sample Rate PCM Audio Data
Supports SACD Bit Stream and External Digital Filter Interface
Accepts a Wide Range of PCM Sample Rates Including: 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, 96 kHz, and 192 kHz
Multibit Sigma-Delta Modulator with "Perfect Differential Linearity Restoration" for Reduced Idle Tones and Noise Floor
Data Directed Scrambling DAC—Low Sensitivity to Jitter
Supports SACD Playback with "Bit Expansion" Filter
Differential Current Output for Optimum Performance
8.64 mA p-p Differential Output
120 dB SNR/DNR (not muted) at 48 kHz Sample Rate (A-Weighted Stereo)
123 dB SNR/DNR (Mono)
–110 dB THD + N
110 dB Stop-Band Attenuation with ±0.0002 dB Pass-Band Ripple
8× Oversampling Digital Filter
On-Chip Clickless Volume Control
Supports SACD-Mute Pattern Detection
Supports 64 f_S/128 f_S DSD SACD with Phase Mode
Internal Digital Filter Pass-Through for External Filter
Master Clock: 256 f_S, 512 f_S, 768 f_S
Hardware and Software Controllable Clickless Mute
Serial (SPI) Control for Serial Mode, Number of Bits, Sample Rate, Volume, Mute, De-Emphasis, Mono Mode
Digital De-Emphasis for 32 kHz, 44.1 kHz, and 48 kHz Sample Rates
Flexible Serial Data Port with Right-Justified, Left-Justified, I²S, and DSP Modes
28-Lead SSOP Plastic Package

APPLICATIONS

High End DVD Audio
SACD
CD
Home Theater Systems
Automotive Audio Systems
Sampling Musical Keyboards
Digital Mixing Consoles
Digital Audio Effects Processors

FUNCTIONAL BLOCK DIAGRAM



PRODUCT OVERVIEW

The AD1955 is a complete, high performance, single-chip, stereo digital audio playback system. It is comprised of a multibit sigma-delta modulator, high performance digital interpolation filters, and continuous-time differential current output DACs. Other features include an on-chip clickless stereo attenuator and mute capability, programmed through an SPI compatible serial control port. The AD1955 is fully compatible with all known DVD audio formats including 192 kHz as well as 96 kHz sample frequencies and 24 bits. It is also backward compatible by supporting 50 µs/15 µs digital de-emphasis intended for "redbook" compact discs, as well as de-emphasis at 32 kHz and 48 kHz sample rates.

The AD1955 has a very flexible serial data input port that allows for glueless interconnection to a variety of ADCs, DSPs, SACD decoders, external digital filters, AES/EBU receivers, and

(continued on page 12)

REV. 0

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AD1955–SPECIFICATIONS

TEST CONDITIONS
(Unless otherwise noted.)

Analog Supply Voltages (AV_{DD}) . . . . . 5 V
Digital Supply Voltages (DV_{DD}) . . . . . 5 V
Reference Current (I_{REF}) . . . . . 0.960 mA
Ambient Temperature . . . . . 25°C
Input Clock . . . . . 12.288 MHz
Input Signal . . . . . 984.375 Hz, 0 dB Full Scale
Input Sample Rate . . . . . 48 kHz
Measurement Bandwidth . . . . . 20 Hz to 20 kHz
Word Width . . . . . 24 Bits
Load Capacitance . . . . . 100 pF
Load Impedance . . . . . 47 kΩ
Input Voltage HI . . . . . 2.4 V
Input Voltage LO . . . . . 0.8 V

ANALOG PERFORMANCE (See figures. I_{REF} = 0.960 mA, V_{BIAS} = 2.80 V.)

Parameter	Min	Typ	Max	Unit
Resolution		24		Bits
SIGNAL-TO-NOISE RATIO (20 Hz to 20 kHz)*				
Differential Output (A-Weighted, RMS) (Stereo)		120	114	dB
Differential Output (A-Weighted, RMS) (Mono)		123		dB
Single-Ended (A-Weighted, RMS) (Stereo)		119		dB
DYNAMIC RANGE (20 Hz to 20 kHz, –60 dB Input)*				
Differential Output (A-Weighted, RMS) (Stereo)		120	114	dB
Differential Output (A-Weighted, RMS) (Mono)		123		dB
Single-Ended (A-Weighted, RMS) (Stereo)		119		dB
Total Harmonic Distortion + Noise (Stereo) at 0 dBFS		–110	–102.5	dB
ANALOG OUTPUTS				
Differential Output Range (Full Scale)		8.64		mA p-p
Output Capacitance at Each Output Pin			100	pF
Output Bias Current, Each Output		–3.24		mA
Out-of-Band Energy (0.5 × f_S to 100 kHz)			–90	dB
Reference Voltage	2.245	2.39	2.505	V
DC ACCURACY				
Gain Error			±6	%
Interchannel Gain Mismatch		0.01	0.26	dB
Gain Drift		25		ppm/°C
Interchannel Crosstalk (EIAJ Method)		–125		dB
Interchannel Phase Deviation		±0.1		Degrees
Mute Attenuation		–100		dB
De-Emphasis Gain Error			±0.1	dB

*Measured with Audio Precision System Two Cascade in RMS Mode. Averaging Mode will show approximately 2 dB better performance.

Performance of right and left channels are identical (exclusive of the Interchannel Gain Mismatch and Interchannel Phase Deviation specifications).

Specifications subject to change without notice.

DIGITAL I/O (–40°C to +85°C, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
Input Voltage HI (V_{IH})	2.2			V
Input Voltage LO (V_{IL})			0.8	V
Input Leakage (I_{IH} @ V_{IH} = 2.4 V)	–3		+3	μA
Input Leakage (I_{IL} @ V_{IL} = 0.8 V)	–3		+3	μA
High Level Output Voltage (V_{OH}) I_{OH} = 1 mA	2.4			V
Low Level Output Voltage (V_{OL}) I_{OL} = 1 mA			0.4	V
Input Capacitance			20	pF

Specifications subject to change without notice.

TEMPERATURE

Parameter	Min	Typ	Max	Unit
Specifications Guaranteed		25		°C
Functionality Guaranteed	–40		+85	°C
Storage	–55		+125	°C

Specifications subject to change without notice.

POWER

Parameter	Min	Typ	Max	Unit
SUPPLIES				
Voltage, Digital	4.50	5	5.50	V
Voltage, Analog	4.50	5	5.50	V
Analog Current		20		mA
Analog Current—Reset		20		mA
Digital Current		22		mA
Digital Current—Reset		2		mA
DISSIPATION				
Operation—Both Supplies		210		mW
Operation—Analog Supply		100		mW
Operation—Digital Supply		110		mW
POWER SUPPLY REJECTION RATIO				
1 kHz 300 mV p-p Signal at Analog Supply Pins		–77		dB
20 kHz 300 mV p-p Signal at Analog Supply Pins		–72		dB

Specifications subject to change without notice.

DIGITAL FILTER CHARACTERISTICS

Sample Rate (kHz)	Pass Band (kHz)	Stop Band (kHz)	Stop-Band Attenuation (dB)	Pass-Band Ripple (dB)
44.1	DC–20	24.1–328.7	110	±0.0002
48	DC–21.8	26.23–358.28	110	±0.0002
96	DC–39.95	56.9–327.65	115	±0.0005
192	DC–87.2	117–327.65	95	0/–0.04 (DC – 21.8 kHz) 0/–0.5 (DC – 65.4 kHz) 0/–1.5 (DC – 87.2 kHz)

Specifications subject to change without notice.

SPECIFICATIONS (continued)

GROUP DELAY

Chip Mode	Group Delay Calculation	f_S (kHz)	Group Delay	Unit
INT8× Mode	$5553/(128 \times f_S)$	48	903.8	µs
INT4× Mode	$5601/(64 \times f_S)$	96	911.6	µs
INT2× Mode	$5659/(32 \times f_S)$	192	921	µs

Specifications subject to change without notice.

DIGITAL TIMING (Guaranteed over –40°C to +85°C, AVDD = DVDD = 5.0 V ± 10%.)

Parameter	Description	Min	Unit
t_{DMP}	MCLK Period ($F_{MCLK} = 256 \times F_{LRCLK}$)	50	ns
t_{DML}	MCLK LO Pulsewidth (All Modes)	$0.4 \times t_{DMP}$	ns
t_{DMH}	MCLK HI Pulsewidth (All Modes)	$0.4 \times t_{DMP}$	ns
t_{DBH}	BCLK/EF_BCLK High	20	ns
t_{DBL}	BCLK/EF_BCLK Low	20	ns
t_{DBP}	BCLK/EF_BCLK Period	60	ns
t_{DLS}	LRCLK/EF_WCLK Setup	0	ns
t_{DLH}	LRCLK Hold (DSP Serial Port Mode Only)	15	ns
t_{DWH}	EF_WCLK High	20	ns
t_{DWL}	EF_WCLK Low	20	ns
t_{DDS}	SDATA/EF_LDATA/EF_RDATA Setup	0	ns
t_{DDH}	SDATA/EF_LDATA/EF_RDATA Hold	20	ns
t_{DPHS}	DSD_PHASE Setup	20	ns
t_{DSDS}	DSD_DATA Setup	5	ns
t_{DSDH}	DSD_DATA Hold	5	ns
t_{DSKP}	DSD_SCLK Period	60	ns
t_{DSKH}	DSD_SCLK High	20	ns
t_{DSKL}	DSD_SCLK Low	20	ns
t_{DMP}	CCLK Period	50	ns
t_{DML}	CCLK LO Pulsewidth	15	ns
t_{DMH}	CCLK HI Pulsewidth	10	ns
t_{CLS}	CLATCH Setup	0	ns
t_{CLH}	CLATCH Hold	15	ns
t_{CDS}	CDATA Setup	0	ns
t_{CDH}	CDATA Hold	5	ns
t_{RSTL}	RST LO Pulsewidth	10	ns

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Min	Max	Unit
DV_{DD} to DGND	–0.3	6	V
AV_{DD} to AGND	–0.3	6	V
Digital Inputs	DGND – 0.3	DV_{DD} + 0.3	V
Analog Outputs	AGND – 0.3	AV_{DD} + 0.3	V
AGND to DGND	–0.3	+0.3	V
Reference Voltage		$(AV_{DD} + 0.3)/2$	
Soldering		300	°C
		10	sec

*Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE CHARACTERISTICS

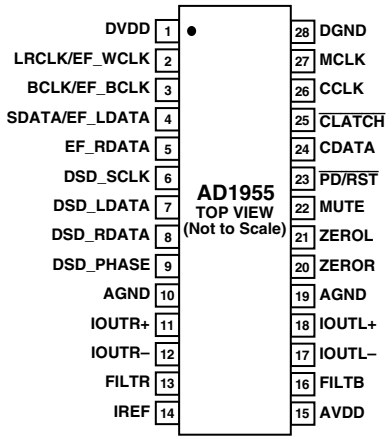
Package	Typ	Unit
θ_{JA} (Thermal Resistance [Junction-to-Ambient])	109.0	°C/W
θ_{JC} (Thermal Resistance [Junction-to-Case])	39.0	°C/W

ORDERING GUIDE

Model	Temperature	Package Description	Package Option*
AD1955ARS	–40°C to +85°C	28-Lead SSOP	RS-28
AD1955ARSRL	–40°C to +85°C	28-Lead SSOP	RS-28 on 13" Reels
EVAL-AD1955EB		Evaluation Board	

*RS = Shrink Small Outline Package

PIN CONFIGURATION

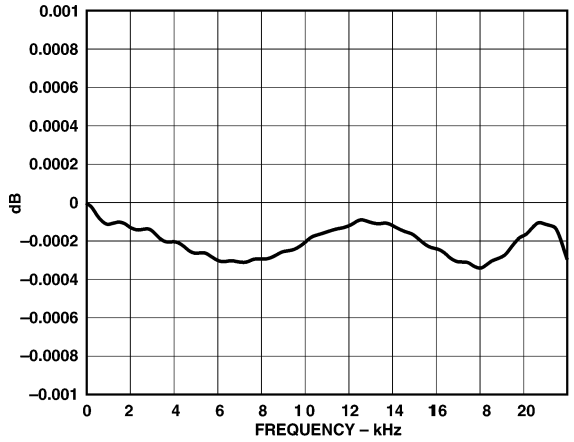


CAUTION

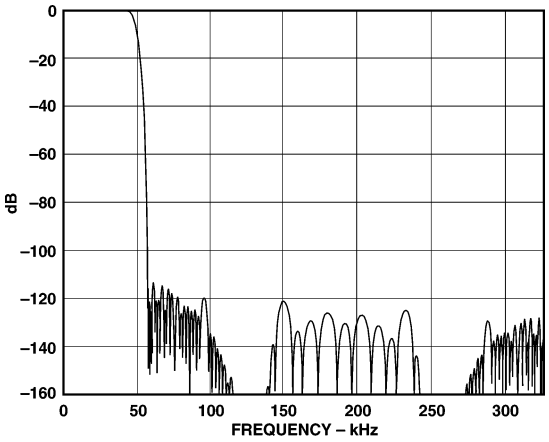
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1955 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

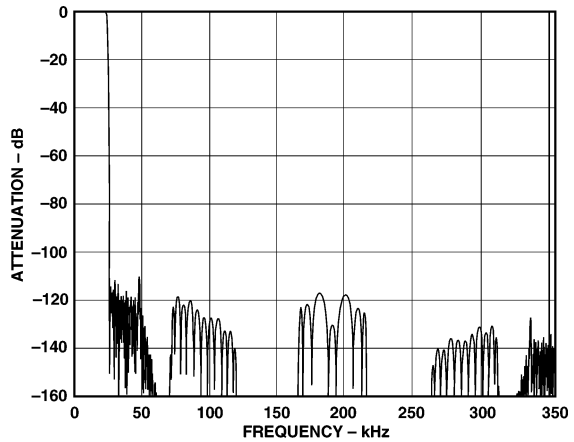
Pin No.	I/O	Mnemonic	Description
1		DVDD	Digital Power Supply Connected to Digital 5 V Supply
2	Input	LRCLK/EF_WCLK	Left/Right Clock Input for Input Data in PCM Mode Word Clock in External Filter Mode
3	Input	BCLK/EF_BCLK	Bit Clock Input for Input Data in PCM Mode Bit Clock Input in External Filter Mode
4	Input	SDATA/EF_LDATA	MSB First, Twos Complement Serial Audio Data Two Channel (left and right), 16-Bit to 24-Bit Data in PCM Mode Left Channel Data in External Filter Mode
5	Input	EF_RDATA	Not used in PCM Mode Right channel data in External Filter Mode
6	I/O	DSD_SCLK	Serial Clock Input for DSD Data. This clock should be 64 × 44.1 kHz, 2.8224 MHz or 128 × 44.1 kHz, 5.6448 MHz in Normal Mode, 128 × 44.1 kHz, 5.6448 MHz or 256 × 44.1 kHz, 11.2896 MHz in Phase Mode.
7	Input	DSD_LDATA	DSD Left Channel Data Input
8	Input	DSD_RDATA	DSD Right Channel Data Input
9	I/O	DSD_PHASE	DSD Phase Reference Signal. This clock should be 64 × 44.1 kHz, 2.8224 MHz. If not used, this pin should be connected low.
10		AGND	Analog Ground
11	Output	IOUTR+	Right Channel Positive Analog Output
12	Output	IOUTR–	Right Channel Negative Analog Output
13	Output	FILTR	Voltage Reference Filter Capacitor Connection. Bypass and decouple the voltage reference with parallel 10 µF and 0.1 µF capacitors to AGND.
14		IREF	Connection Point for External Bias Resistor
15		AVDD	Analog Power Supply Connected to Analog 5 V Supply
16	Output	FILTB	Filter Capacitor Connection with Parallel 10 µF and 0.1 µF Capacitors to AGND
17	Output	IOUTL–	Left Channel Negative Analog Output
18	Output	IOUTL+	Left Channel Positive Analog Output
19		AGND	Analog Ground
20	Output	ZEROR	Right Channel Zero Flag Output. This pin goes high when the right channel has no signal input or the DSD mute pattern is detected.
21	Output	ZEROL	Left Channel Zero Flag Output. This pin goes high when the left channel has no signal input or the DSD mute pattern is detected.
22	Input	MUTE	Mute. Assert high to mute both stereo analog outputs. Deassert low for normal operation.
23	Input	$\overline{\text{PD/RST}}$	Power Down/Reset. The AD1955 is placed in a reset state and the digital circuitry is powered down when this pin is held low. The AD1955 is reset on the rising edge of this signal. The serial control port registers are reset to the default values. Connect high for normal operation.
24	Input	CDATA	Serial Control Input, MSB First, Containing 16 Bits of Unsigned Data. Used for specifying control information and channel-specific attenuation.
25	Input	$\overline{\text{CLATCH}}$	Latch Input for Control Data
26	Input	CCLK	Clock Input for Control Data. Control input data must be valid on the rising edge of CCLK. CCLK may be continuous or gated.
27	Input	MCLK	Master Clock Input. Connect to an external clock source.
28		DGND	Digital Ground



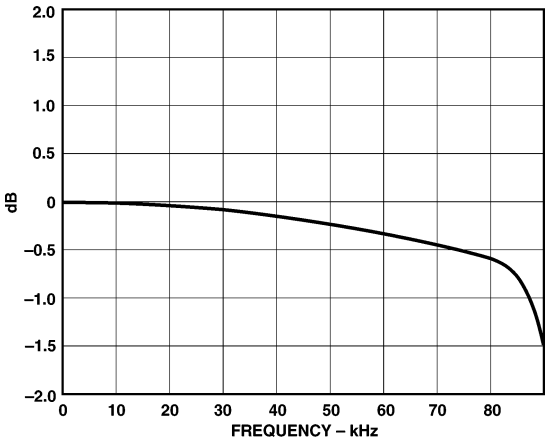
TPC 1. Pass-Band Response, 8× Mode, 48 kHz Sample Rate



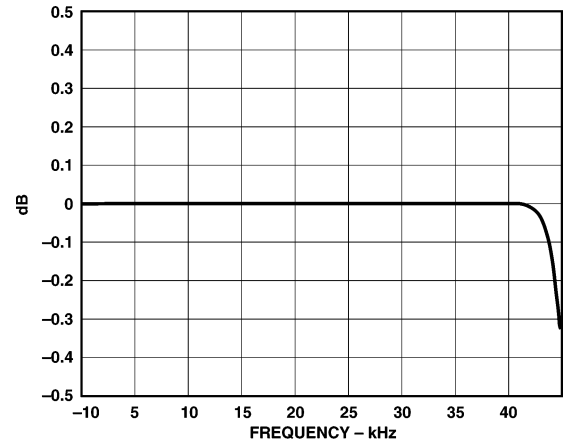
TPC 4. Complete Response, 4× Mode, 96 kHz Sample Rate



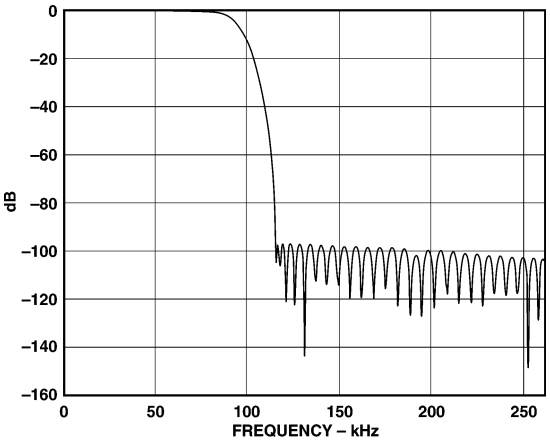
TPC 2. Complete Response, 8× Mode, 48 kHz Sample Rate



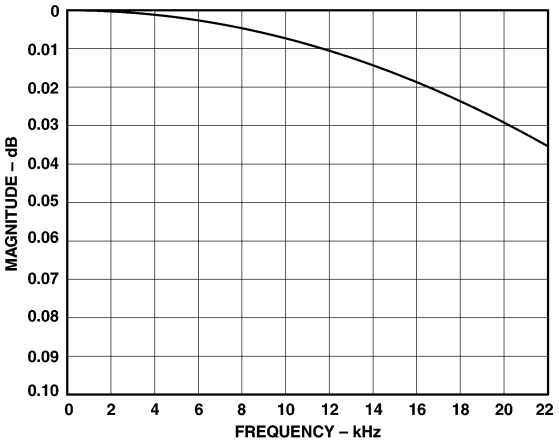
TPC 5. Pass-Band Response, 2× Mode, 192 kHz Sample Rate



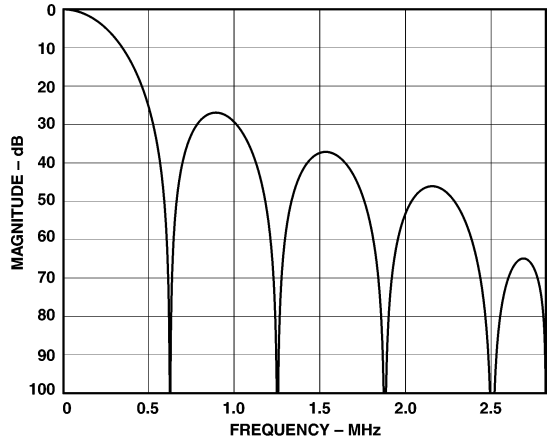
TPC 3. 44 kHz Pass-Band Response 4× Mode, 96 kHz Sample Rate



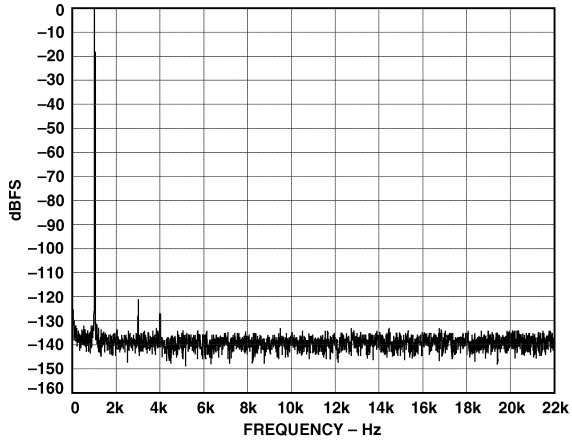
TPC 6. Complete Response, 2× Mode, 192 kHz Sample Rate



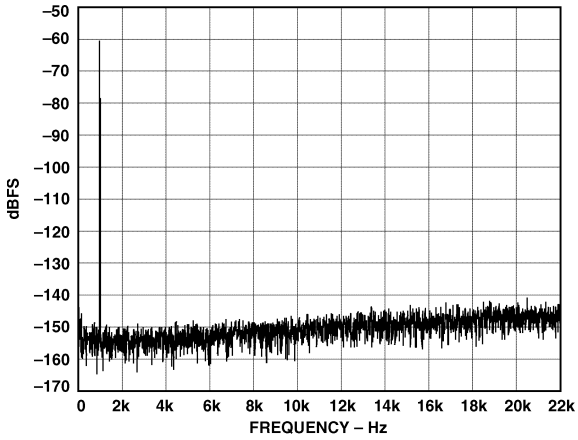
TPC 7. DSD Digital Filter Pass Band



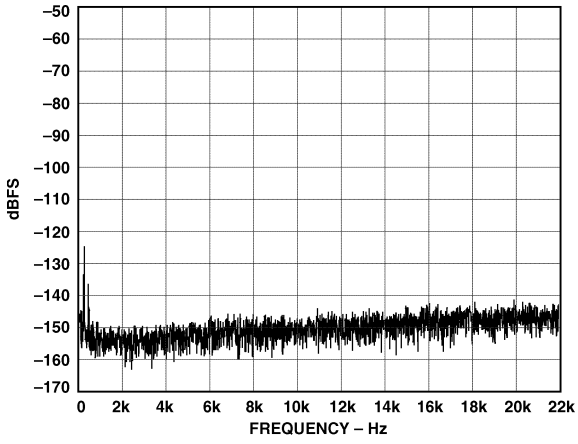
TPC 8. DSD Digital Filter Response, Input Sample Rate = 2.8224 MHz



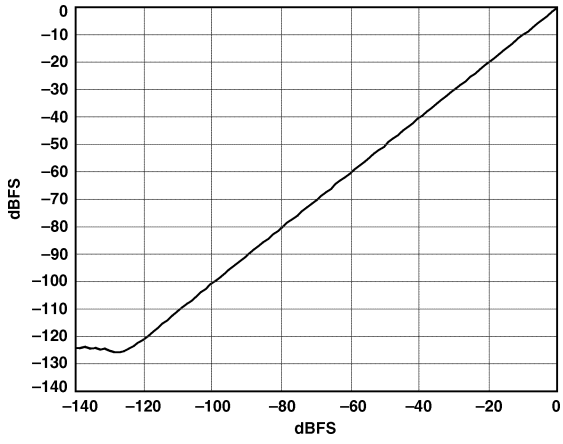
TPC 9. FFT Plot, THD + N = –110 dBFS, PCM SR = 48 kHz, 0 dBFS @ 1 kHz



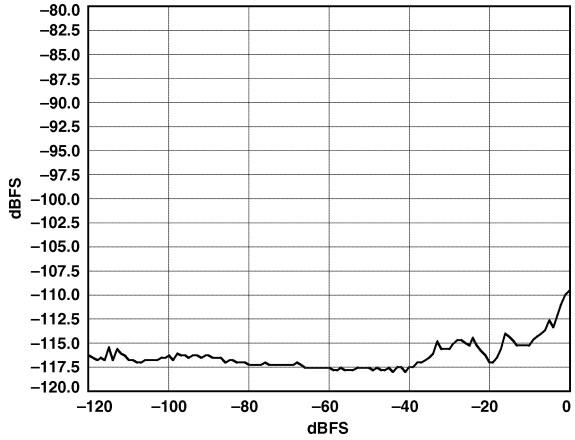
TPC 10. FFT Plot, DNR = 121 dBFS (A-Weight), PCM SR = 48 kHz, –60 dBFS @ 1 kHz



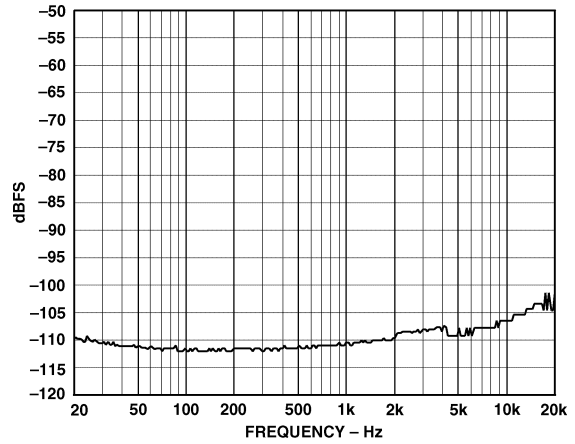
TPC 11. FFT Plot, SNR = 121 dBFS (A-Weight), PCM SR = 48 kHz with Zero Input



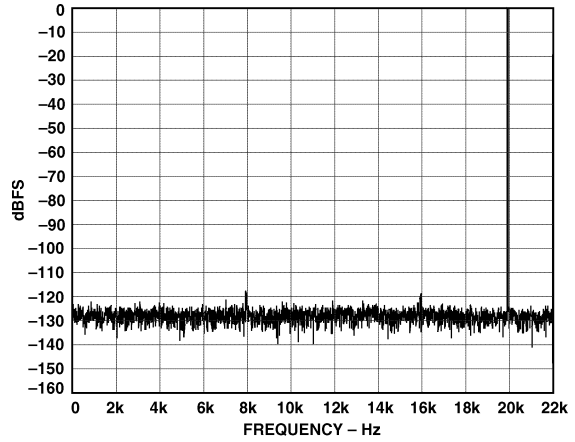
TPC 12. Linearity, PCM SR = 48 kHz, 0 dBFS to –140 dBFS Input @ 200 Hz



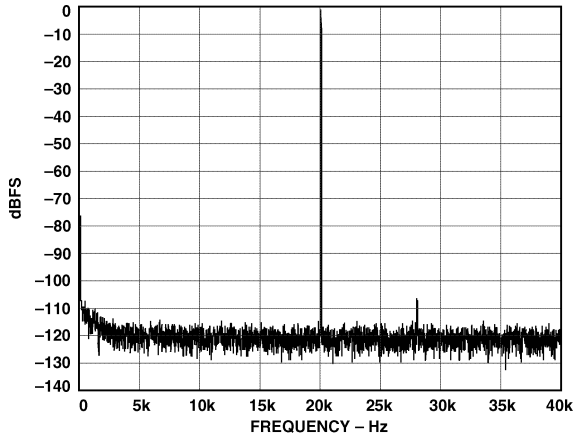
TPC 13. THD + N vs. Amplitude Plot, PCM SR = 48 kHz, 0 dBFS to –120 dBFS Input @ 1 kHz



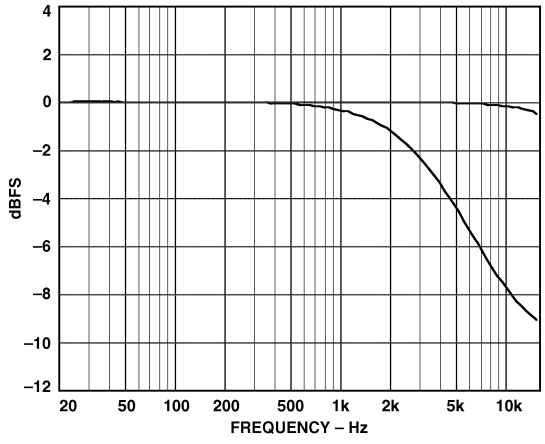
TPC 14. THD + N vs. Frequency Plot, PCM SR = 48 kHz, 0 dBFS Input



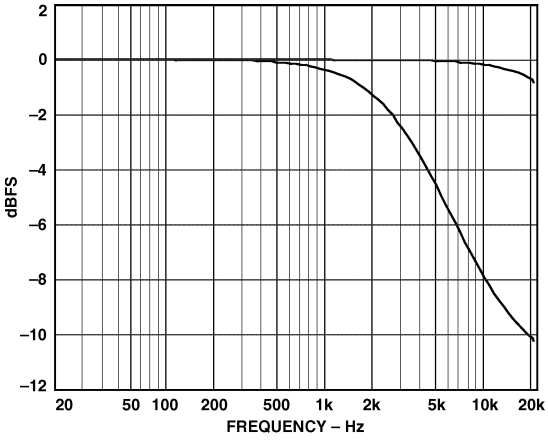
TPC 15. FFT Plot, PCM SR = 48 kHz, 0 dBFS @ 20 kHz, BW = 22 kHz



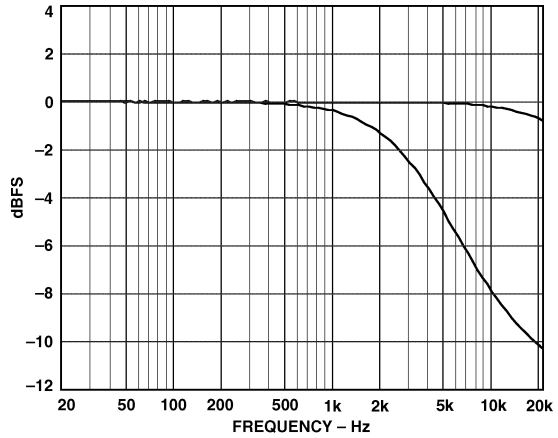
TPC 16. Wideband FFT Plot, PCM SR = 48 kHz, 0 dBFS @ 20 kHz



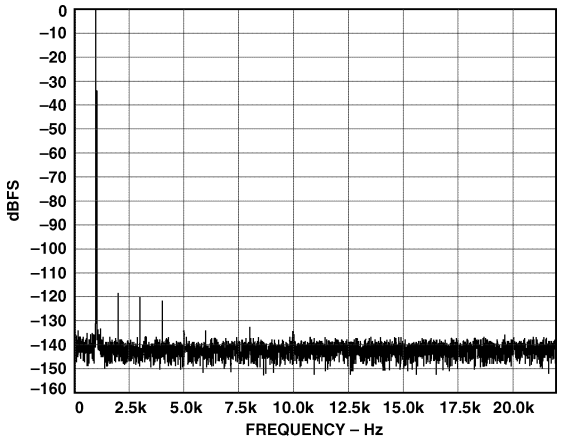
TPC 17. De-emphasis Frequency Response, PCM SR = 32 kHz, 0 dBFS Input



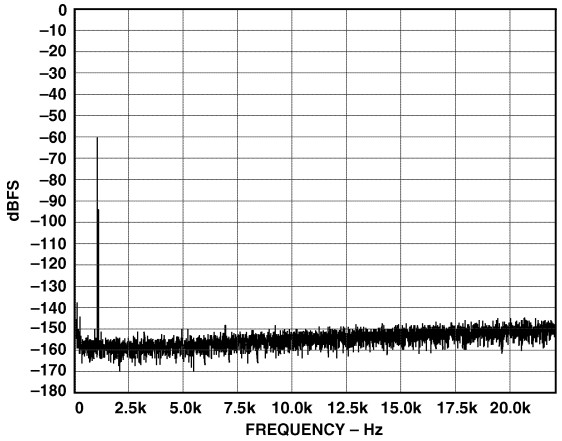
TPC 18. De-emphasis Frequency Response, PCM SR = 44.1 kHz, 0 dBFS Input



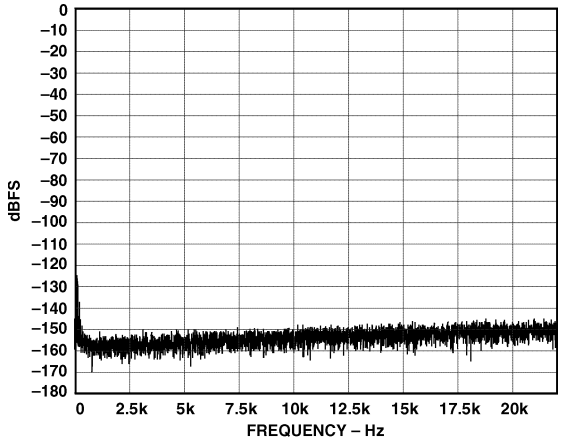
TPC 19. De-emphasis Frequency Response, PCM SR = 48 kHz, 0 dBFS Input



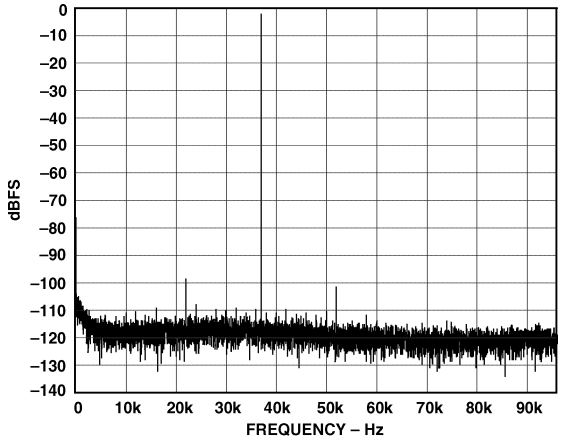
TPC 20. FFT Plot, PCM SR = 96 kHz, 0 dBFS @ 1 kHz, BW = 22 kHz



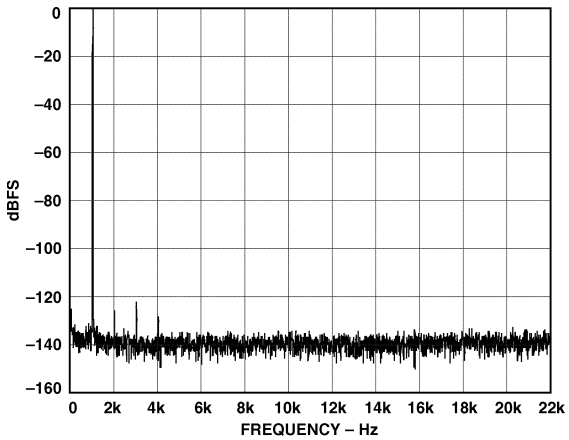
TPC 21. FFT Plot, PCM SR = 96 kHz, –60 dBFS @ 1 kHz, BW = 22 kHz



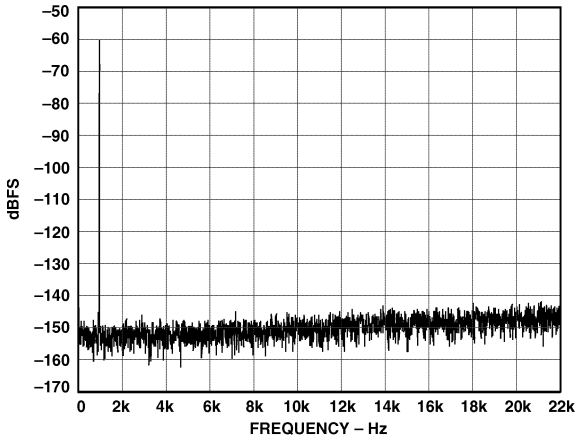
TPC 22. FFT Plot, PCM SR = 96 kHz, Zero Input, BW = 22 kHz



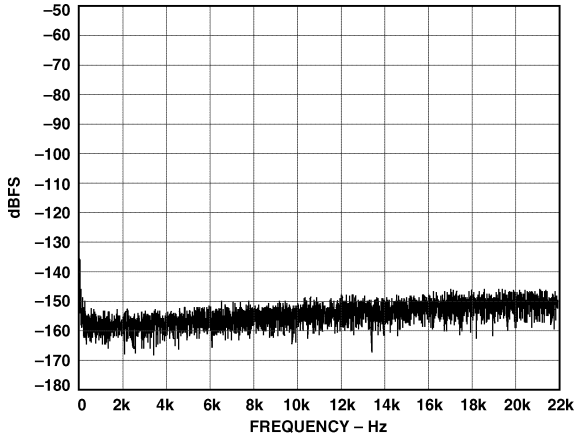
TPC 23. Wideband FFT Plot, PCM SR = 96 kHz, 0 dBFS Input @ 37 kHz



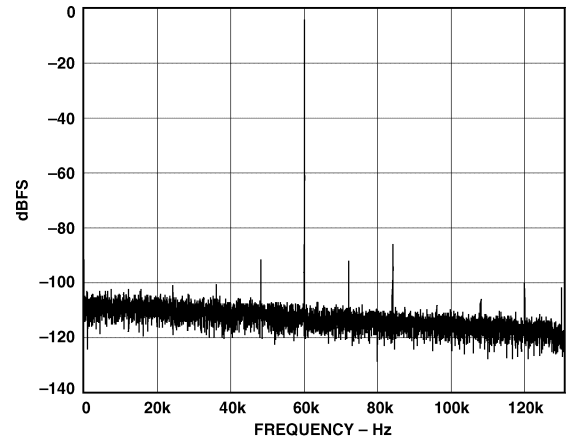
TPC 24. FFT Plot, PCM SR = 192 kHz, 0 dBFS Input @ 1 kHz



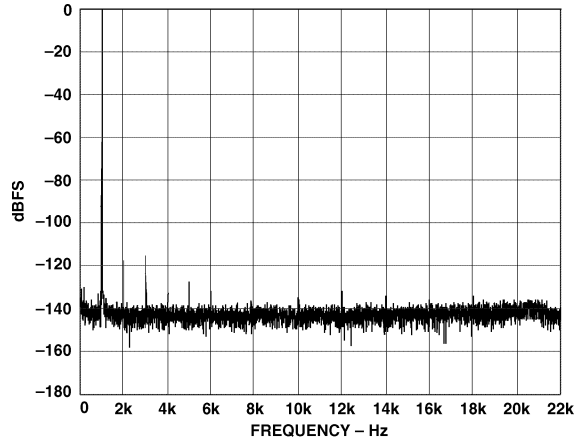
TPC 25. FFT Plot, PCM SR = 192 kHz, –60 dBFS Input @ 1 kHz



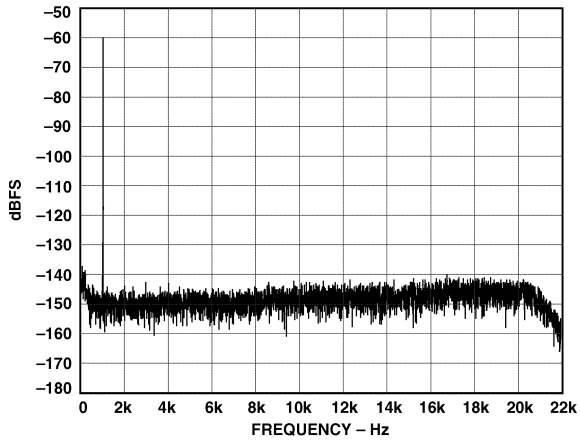
TPC 26. FFT Plot, PCM SR = 192 kHz, Zero Input



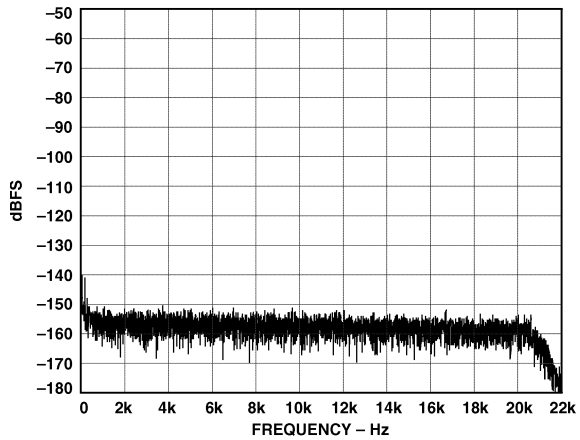
TPC 27. Wideband FFT Plot, PCM SR = 192 kHz, 0 dBFS @ 60 kHz



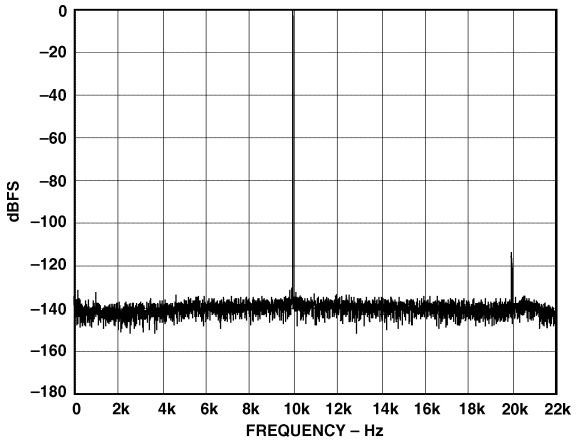
TPC 28. FFT Plot, 64 × f_S DSD, SR = 44.1 kHz, 0 dBFS @ 1 kHz



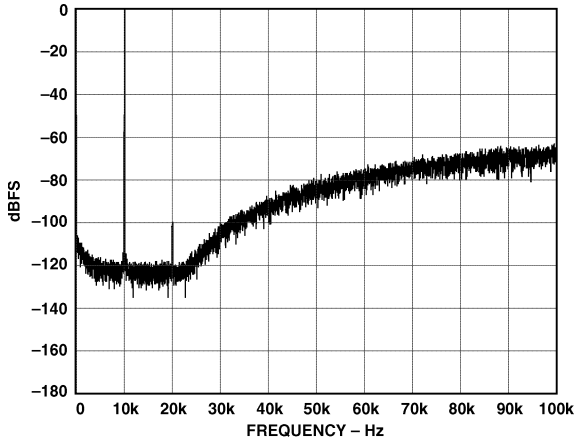
TPC 29. FFT Plot, 64 × f_S DSD, SR = 44.1 kHz, –60 dBFS @ 1 kHz



TPC 30. FFT Plot, 64 × f_S DSD, SR = 44.1 kHz, Zero Input



TPC 31. FFT Plot, 64 × f_S DSD, SR = 44.1 kHz, 0 dBFS @ 10 kHz



TPC 32. Wideband FFT Plot, 64 × f_S DSD, SR = 44.1 kHz, 0 dBFS @ 10 kHz

(continued from page 1)
sample rate converters. The AD1955 can be configured in left-justified, I²S, right-justified, or DSP serial port compatible modes. It can support MSB first, twos complement format, 16, 18, 20, and 24 bits in all standard PCM modes. The AD1955 also has an interface for SACD playback and an external digital filter interface for use with an external digital interpolation filter or HDCD decoder. The AD1955 uses a 5 V power supply. It is fabricated on a single monolithic integrated circuit and is housed in a 28-lead SSOP package for operation over the temperature range –40°C to +85°C.

OPERATING FEATURES

Serial Data Input Port

The AD1955's flexible serial data input port accepts standard PCM audio data and external digital filter output data in twos complement, MSB-first format in PCM/External Digital Filter Mode, and a dedicated SACD serial port accepts DSD bit stream data in SACD Mode. If the PCM Mode is selected by Control Register 0 Bits 12 and 13, the left channel data field always precedes the right channel data field. The serial data format and word length in PCM Mode are set by the mode select bits (Bits 4 and 5 and Bits 2 and 3, respectively) in the SPI control register.

In all data formats except for the Right-Justified Mode, the serial port will accept an arbitrary number of bits up to a limit of 24 (extra bits will not cause an error, but they will be truncated internally). In Right-Justified Mode, Control Register 0, Bits 2 and 3 are used to set the word length to 16, 18, 20, or 24 bits. The default on power up is 24-bit, I²S.

In the External Digital Filter Mode, selected by Control Register 0 Bits 12 and 13, Bits 2 and 3 are used to set the word length to 16, 18, 20, or 24 bits and the format is set with Bits 4 and 5. For a burst-mode clock, the format should be set to left-justified. DSP Mode is not used. The LRCLK is always falling-edge active. The default on power-up is 24-bit mode in PCM and External Digital Filter Mode.

In SACD Mode, selected by Control Register 0 Bits 12 and 13, the SACD port will accept a DSD bit stream.

When the SPI Control Port is not being used, the SPI pins (24, 25, and 26) should be tied to DGND or DVDD.

Serial Data Format in PCM Mode

The supported formats are shown in Figure 1. For detailed timing, see Figure 2.

In Left-Justified Mode, LRCLK is high for the left channel and low for the right channel. Data should be valid on the rising edge of BCLK. The MSB is left-justified to an LRCLK transition, with no MSB delay.

In I²S Mode, LRCLK is low for the left channel and high for the right channel. Data should be valid on the rising edge of BCLK. The MSB is left-justified to an LRCLK transition but with a single BCLK period delay.

In DSP serial port mode, LRCLK must pulse high for at least one bit clock period before the MSB of the left channel is valid, and LRCLK must pulse high again for at least one bit clock period before the MSB of the right channel is valid. Data should be valid on the falling edge of BCLK. The DSP serial port mode can be used with any word length up to 24 bits.

In this mode, it is the responsibility of the DSP to ensure that the left data is transmitted with the first LRCLK pulse after RESET, and that synchronism is maintained from that point forward.

In Right-Justified Mode (16 bits shown), LRCLK is high for the left channel and low for the right channel. Data should be valid on the rising edge of BCLK.

In normal operation, there are 64 bit clocks per frame (or 32 per half-frame). When the SPI word length control bits (Bits 2 and 3 in Control Register 0) are set to 24 bits (0:0), the serial port will begin to accept data starting at the eighth bit clock pulse after the LRCLK transition. When the word length control bits are set to 20-bit mode, data is accepted starting at the 12th bit clock position. In 18-bit mode, data is accepted starting at the 14th bit clock position. In 16-bit mode, data is accepted starting at the 16th bit clock position.

Note that the AD1955 is capable of a 32 × f_S BCLK frequency "packed mode" where the MSB is left-justified to an LRCLK transition, and the LSB is right-justified to the next LRCLK transition. LRCLK is high for the left channel, and low for the right channel. Data is valid on the rising edge of BCLK. Packed mode can be used when the AD1955 is programmed in Left-Justified Mode.

Serial Data Format in External Digital Filter Mode
In the External Digital Filter Mode, the AD1955 will accept up to 24-bit serial, twos complement, MSB-first data from an external digital filter, an HDCD decoder, or a general-purpose DSP. If the External Digital Filter Mode is selected by Control Register 0, Bits 12 and 13, Pin 2 to Pin 5 are assigned as the word clock input (EF_WCLK, Pin 2), bit clock input (EF_BCLK, Pin 3), left channel data input (EF_LDATA, Pin 4), and right channel data input (EF_RDATA, Pin 5), respectively, to accept $8f_S$ (48 kHz), $4f_S$ (96 kHz), or $2f_S$ (196 kHz) oversampled data.

Left and right channel data should be valid on the rising edge of EF_BCLK. The mode can be set to Left- or Right-Justified. A burst mode BCLK can be used in Left-Justified Mode.

Serial Data Format in SACD Mode
In the SACD Mode, the AD1955 supports both normal mode or phase modulation mode, which are selected by Control Register 1, Bit 6. If normal mode is selected, DSD_SCLK, DSD_LDATA, and DSD_RDATA are used to interface with DSD decoder chip. In this mode, the DSD data is clocked in the AD1955 using the rising edge of DSD_SCLK with a $64f_S$ rate, 2.8224 MHz. DSD_PHASE pin should be connected LOW.

If Phase Modulation Mode is selected, the DSD_PHASE pin is also used to interface with the DSD decoder. In this mode, a $64f_S$ DSD_PHASE signal is used as a reference signal to receive the data from the decoder. The DSD data is clocked into the AD1955 with a $128f_S$ DSD_SCLK.

The AD1955 can operate as a master or slave device. In Master Mode, the AD1955 will output DSD_SCLK and DSD_PHASE (if in Phase Modulation Mode) to a DSD decoder and will support Normal Mode and Phase Modulation Mode 0. In Slave Mode, the AD1955 will accept DSD_SCLK and DSD_PHASE (if in Phase Modulation Mode) from a DSD decoder and supports all of the normal and phase modulation modes.

When the SACD Port is not being used, the SACD pins (Pins 6, 7, 8, and 9) should be tied to a valid logic level. Please note that there are weak pull-ups (0.6 mA typical) on DSD_SCLK and DSD_PHASE.

Master Clock
The AD1955 must be set to the proper sample rate and master clock rate using Control Registers 0 and 1. The allowable master clock frequencies for each interpolation mode are shown below.

In the External Filter Mode, the AD1955 accepts master clock frequencies depending on the input sample rate as shown below.

In the SACD Mode, the AD1955 accepts a $256f_S$, $512f_S$, or $768f_S$ Master Clock, where f_S is nominally 44.1 kHz. In Slave Mode, by default, the rising edge of DSD_SCLK should coincide with the rising edge of MCLK. Control Register 1, Bit 2 should be set to 1 if the rising edge of DSD_SCLK coincides with the falling edge of MCLK. In Master Mode this bit can be used to select the MCLK edge used to generate the DSD clock outputs.

Zero Detection
When the AD1955 detects that the audio input data is continuously zero during 1024 LRCLK periods in PCM Mode or 8192 LRCLK periods in $8f_S$ External Digital Filter Mode, ZEROL (Pin 21) or ZEROR (Pin 20) is set to active.

When the AD1955 is in SACD Mode, it will detect an SACD mute pattern. If the input bit stream shows a mute pattern for about 22 ms, the AD1955 will set ZEROL (Pin 21) or ZEROR (Pin 20) to active. The outputs can be set to active high or low using Control Register 1, Bit 8.

Reset/Power-Down
The AD1955 will be reset when the $\overline{\text{PD/RST}}$ pin is set low. The part may be powered down using Bit 15, Control Register 0.

Audio Outputs
Active I/V converters should be used, which will hold the DAC outputs at a constant voltage level. Passive I/V conversion should not be used, since the DAC performance will be seriously degraded. For best THD + N performance over temperature, a reference voltage of 2.80 V should be used with the I/V converters. For a lower parts count, the voltage at FILTR can be used. In this instance, THD + N performance at high temperature can be improved by reducing I_{REF}, with an attendant reduction in gain (linear dependence) and DNR/SNR (square-root dependence).

The AD1955 audio outputs sink a current proportional to the input signal, superimposed on a steady bias current. The current-to-voltage (I/V) converters used need to be able to supply this bias current, as well as the signal current, or a resistor or current source can be used to a positive voltage to null this current in order to center the range of the I/V converters.

If pull-up resistors are used to bring the output of the I/V converters to 0 V for maximum headroom and THD balance, as shown in the applications circuits, the following equation can be used:

$$R_{PULLUP} = \left[V_{SUPPLY} - V_{BIAS}\right] / \left[I_{BIAS} + (V_{BIAS} / R_{I/V})\right]$$

PCM Mode

Interpolation Mode	Allowable Master Clock Frequencies (× f_S)								Nominal Input Sample Rate (kHz)
	64	96	128	192	256	384	512	768	
48 kHz (INT 8×) Mode					•		•	•	32, 44.1, 48
96 kHz (INT 4×) Mode			•		•	•			88.2, 96
192 kHz (INT 2×) Mode	•		•	•					176.4, 192

External Filter Mode

Input Sample Rate	Allowable Master Clock Frequencies (× f_S)								Nominal Input Sample Rate (to External Filter) (kHz)
	64	96	128	192	256	384	512	768	
$8 \times f_S$					•		•	•	32, 44.1, 48
$4 \times f_S$			•		•	•			88.2, 96
$2 \times f_S$	•		•	•					176.4, 192

For example, with the stereo circuits given in Figures 7 through 10, this gives:

$$\left[12.0\,V - 2.80\,V\right] / \left[3.24\,mA + \left(2.80\,V / 2.00\,K\right)\right] = 1.98\,k\Omega$$

A 2.00 kΩ resistor is used.

The supply used should be as quiet as possible.

Serial Control Port

The AD1955 has an SPI compatible control port to permit programming the internal control registers. The SPI control port is a 3-wire serial port. Its format is similar to the Motorola SPI format except that the input data-word is 16 bits wide. The serial bit clock may be completely asynchronous to the sample rate of the DAC. The following figure shows the format of the SPI signal Note that the CCLK may be continuous or a 16-clock burst.

SPI REGISTER DEFINITIONS

Table I. DAC Control Register 0

Bit	Description	Value	Definition
15	Power-Down	0 1	Operation Powered Down
14	Mute	0 1	Not Muted Muted
13:12	Data Format	00 01 10 11	PCM External DF SACD Slave SACD Master
11:10	Output Format	00 01 10 11	Stereo Not Allowed Mono Left Mono Right
9:8	PCM Sample Rate	00 01 10 11	48 kHz 96 kHz 192 kHz Reserved
7:6	De-Emphasis Curve Select	00 01 10 11	None 44.1 kHz 32 kHz 48 kHz
5:4	PCM/EF Serial Data Format	00 01 10 11	I^2S Right-Justified DSP Left-Justified
3:2	PCM/EF Serial Data Width	00 01 10 11	24 bits 20 bits 18 bits 16 bits
1:0	SPI Register Address	00	

Default = 0

Table II. DAC Control Register 1

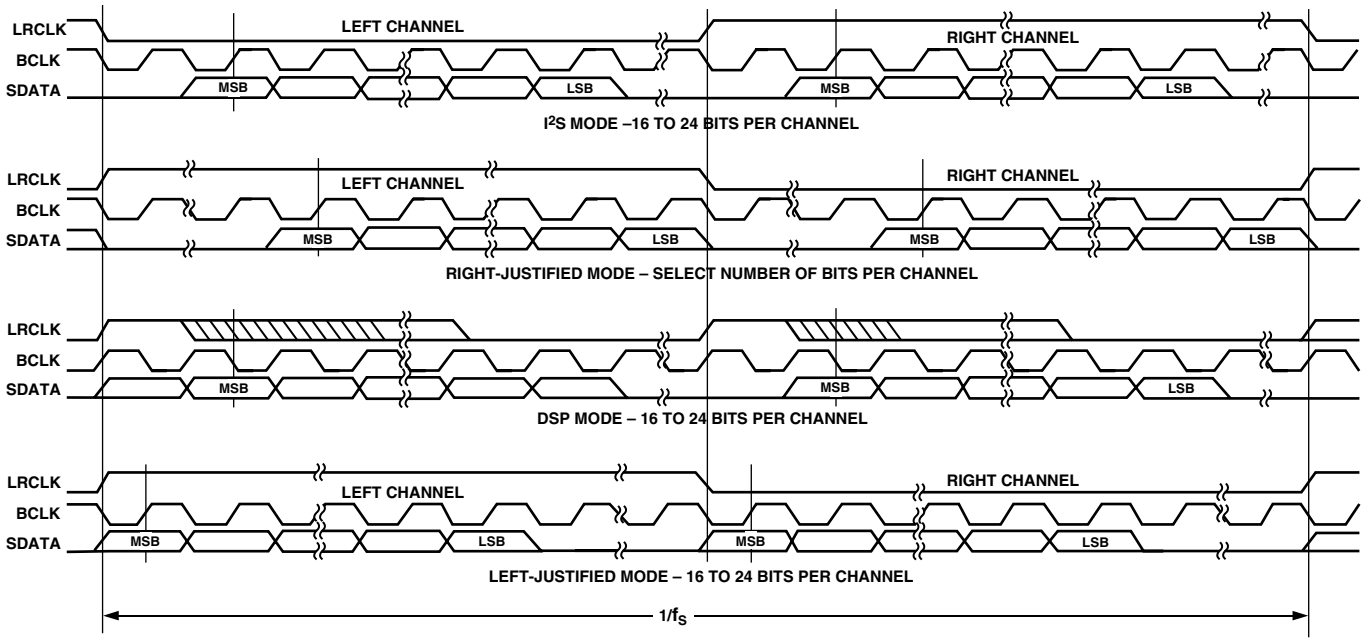
Bit	Description	Value	Definition
10:9	MCLK Mode	00 01 10 11	$256 \times f_S$ $512 \times f_S$ $768 \times f_S$ Reserved
8	Zero Flag Polarity	0 1	Active High Active Low
7	SACD Bit Rate	0 1	$64 \times f_S$ $128 \times f_S$
6	SACD Mode	0 1	Normal Phase Mode
5:4	SACD Phase Select	00 01 10 11	Phase 0 Phase 1 Phase 2 Phase 3
3	SACD Bit Inversion	0 1	Normal Inverted
2	SACD MCLK to BCLK Phase	0 1	Rising Edge Falling Edge
1:0	SPI Register Address	01	

Default = 0

Table III. DAC Volume Registers

Bit	Description	Value	Definition
15:2	Volume	14-Bit Unsigned	
1:0	SPI Register Address	10 11	Left Volume Right Volume

Default = Full Volume



NOTES
1. DSP MODE DOES NOT IDENTIFY CHANNEL.
2. LRCLK NORMALLY OPERATES AT f_S EXCEPT FOR DSP MODE, WHICH IS 2 × f_S.
3. BCLK FREQUENCY IS NORMALLY 64 × LRCLK BUT MAY BE OPERATED IN BURST MODE.

Figure 1. Supported Serial Data Formats

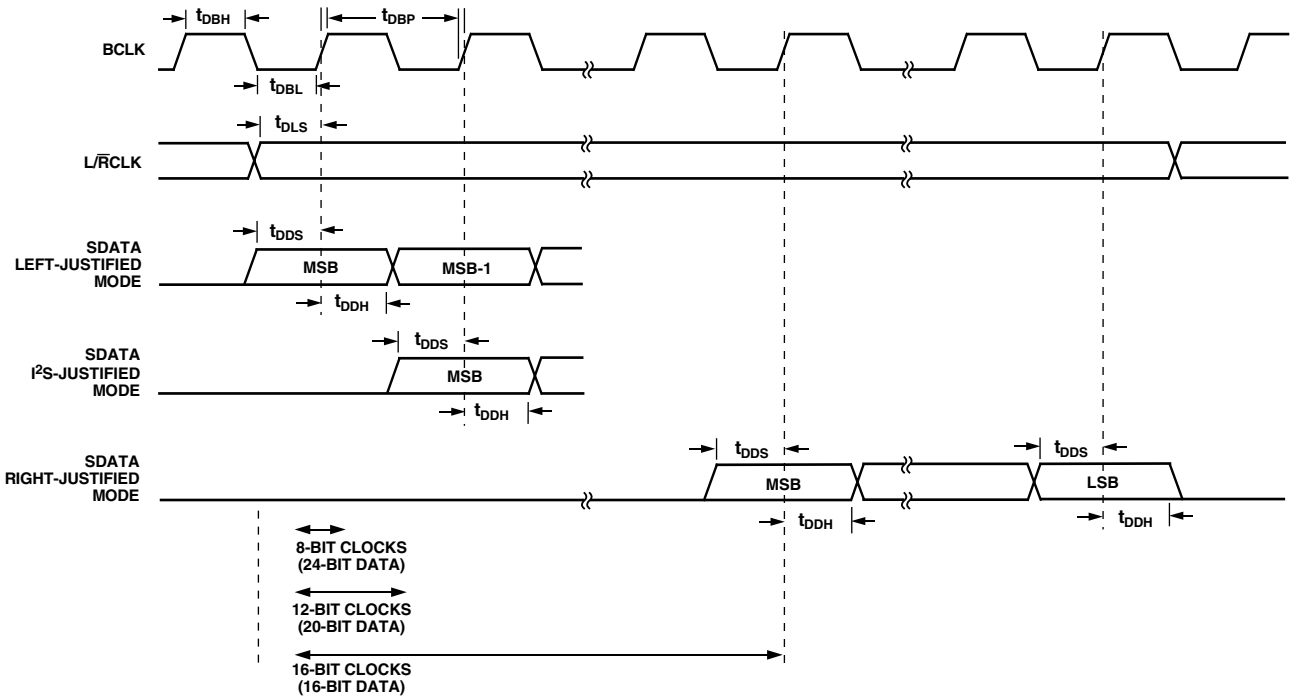


Figure 2. Serial Data Port Timing

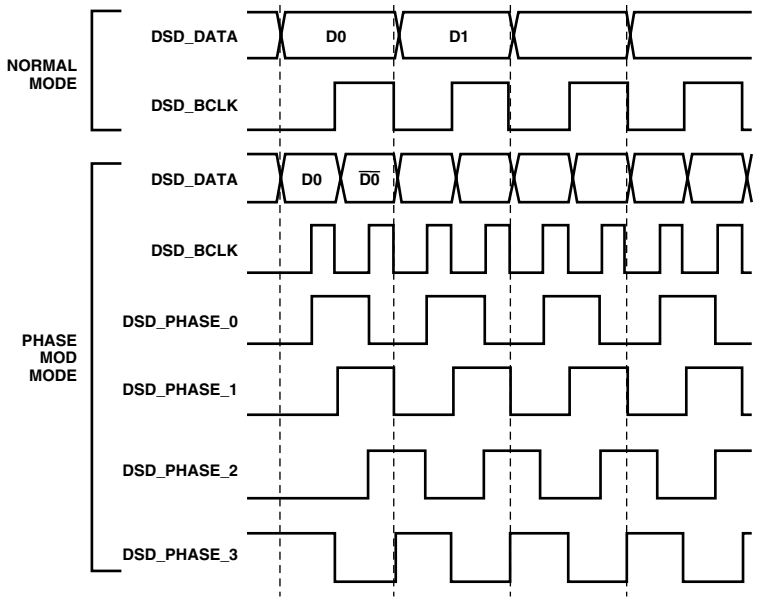


Figure 3. DSD Modes

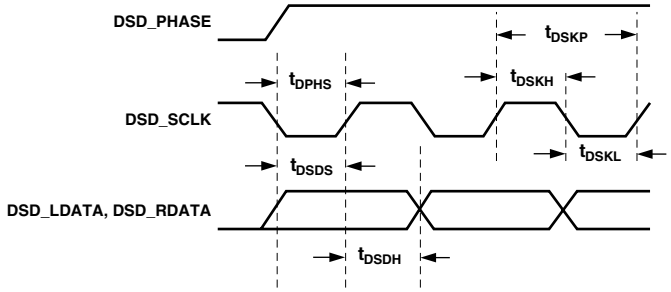


Figure 4. DSD Serial Port Timing

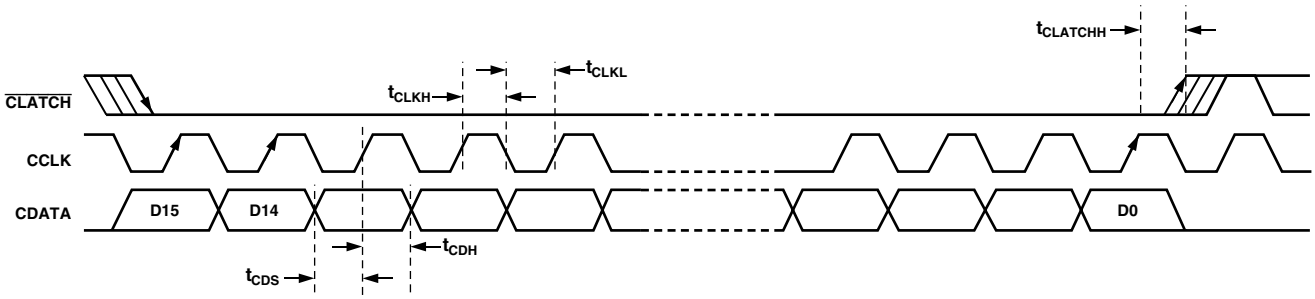


Figure 5. Serial Control Port Timing

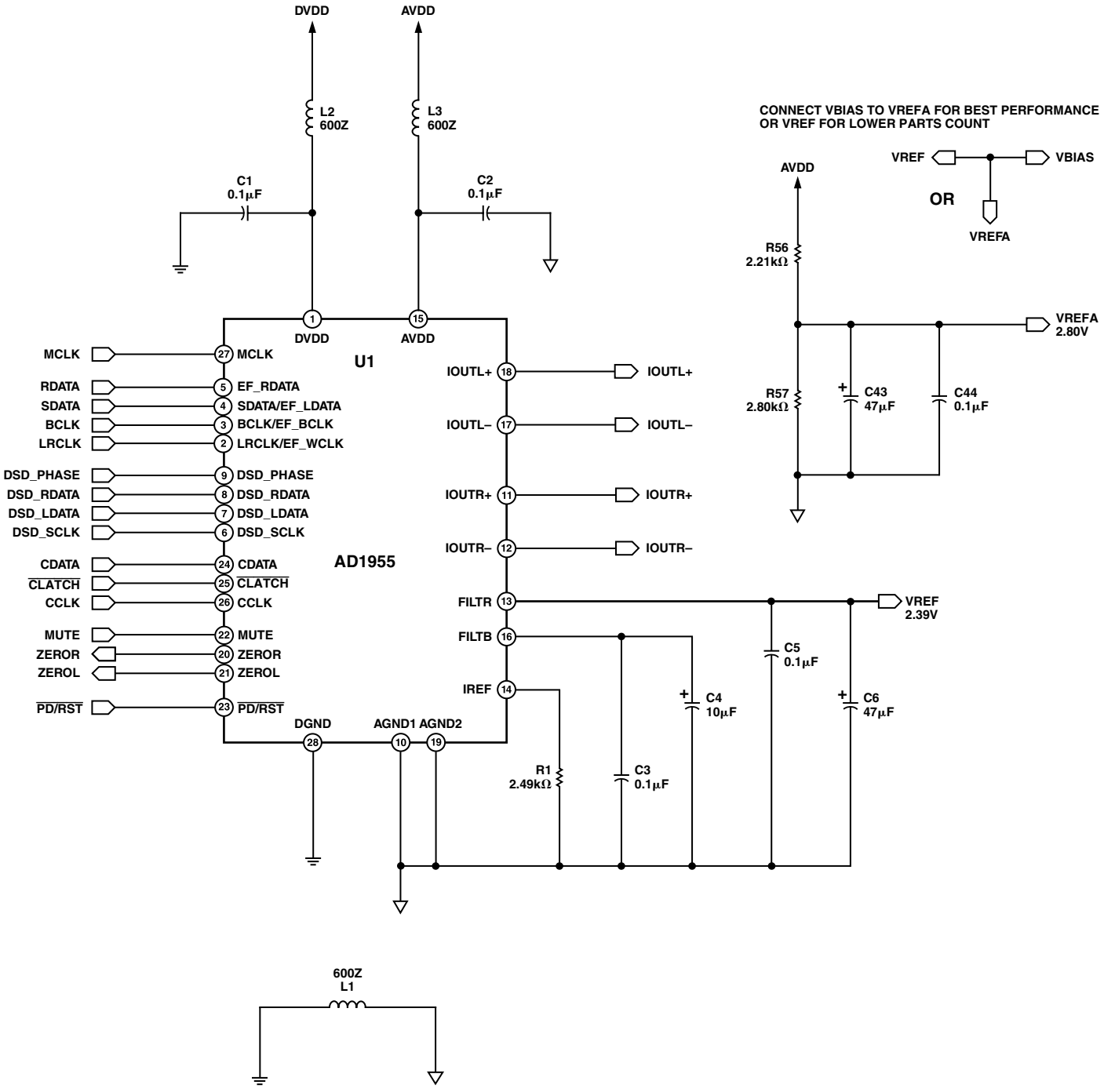


Figure 6. DAC Power Supply and Bypass

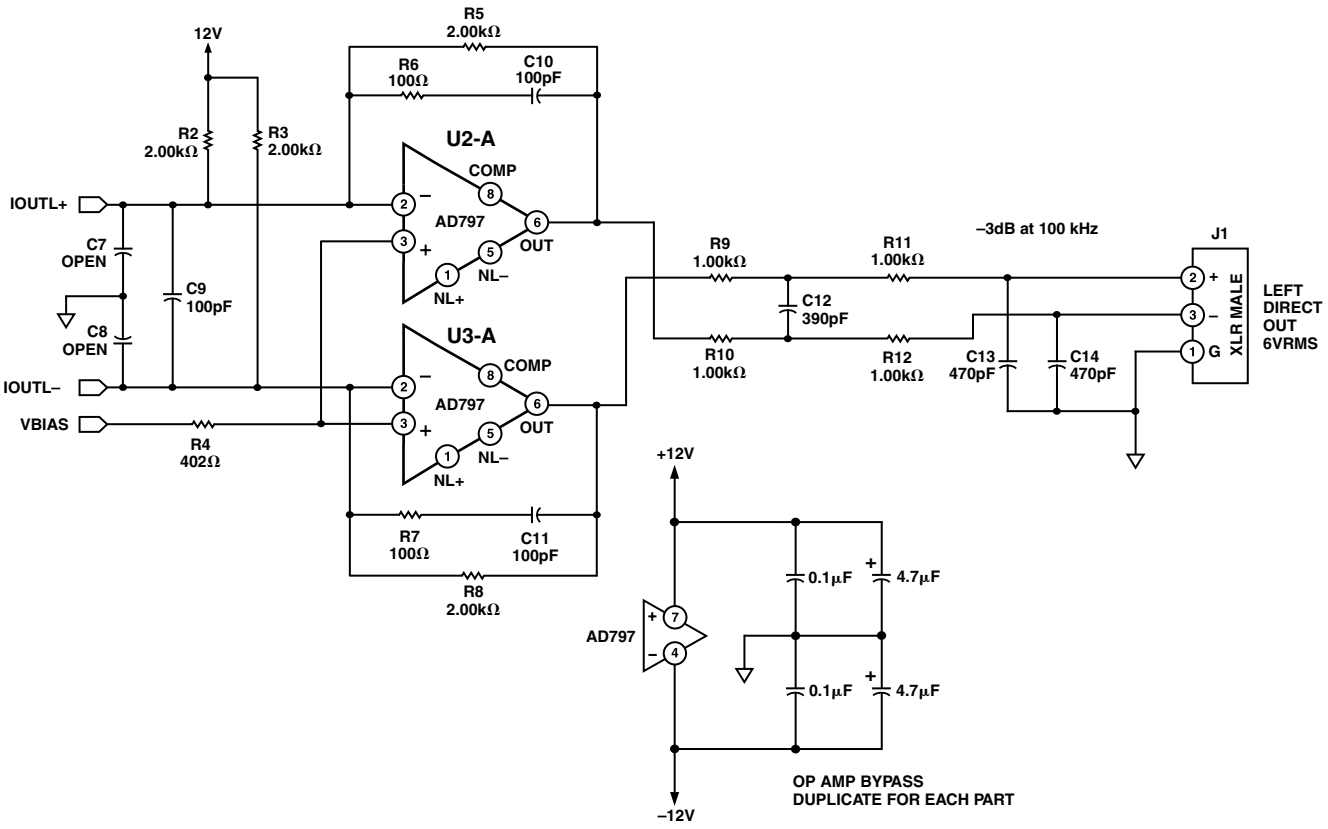


Figure 7. Left Channel Differential Output

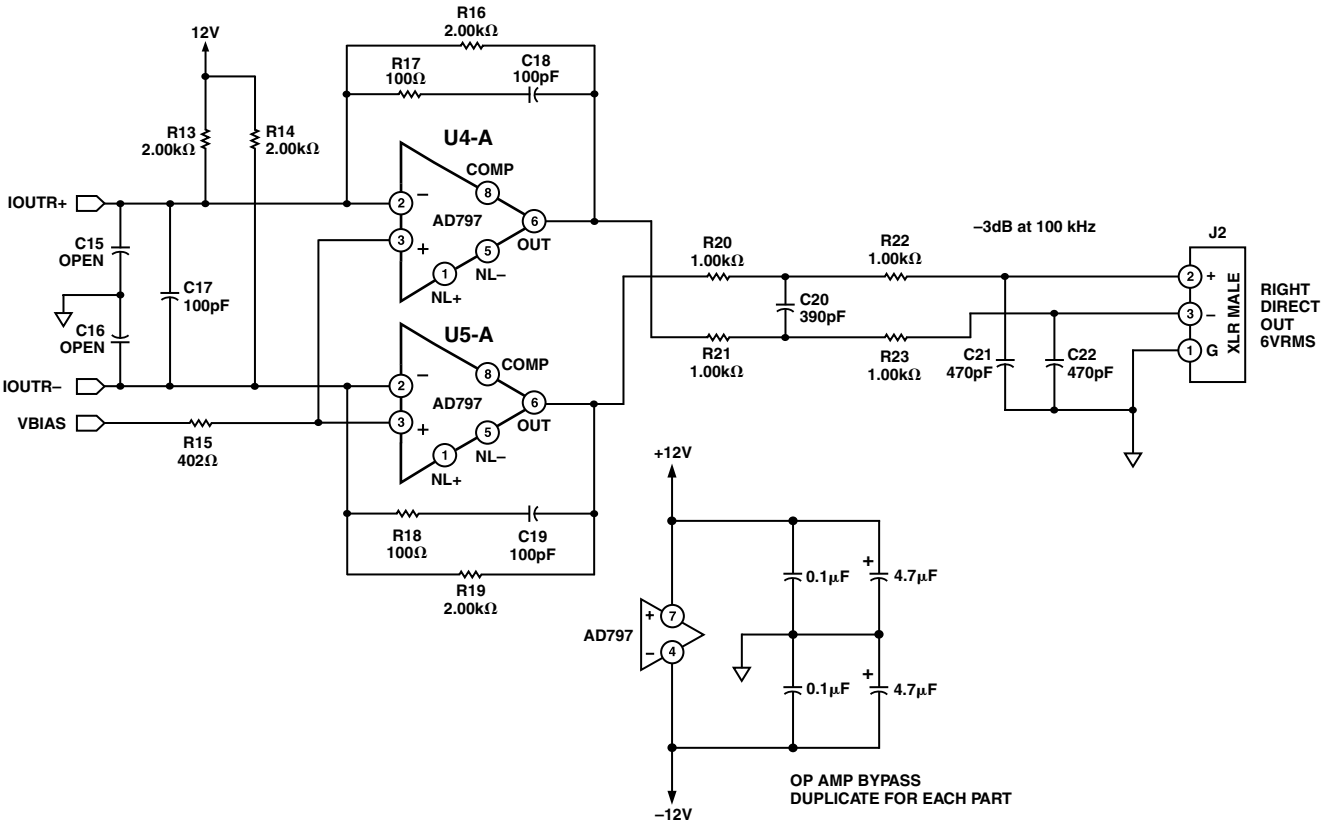


Figure 8. Right Channel Differential Output

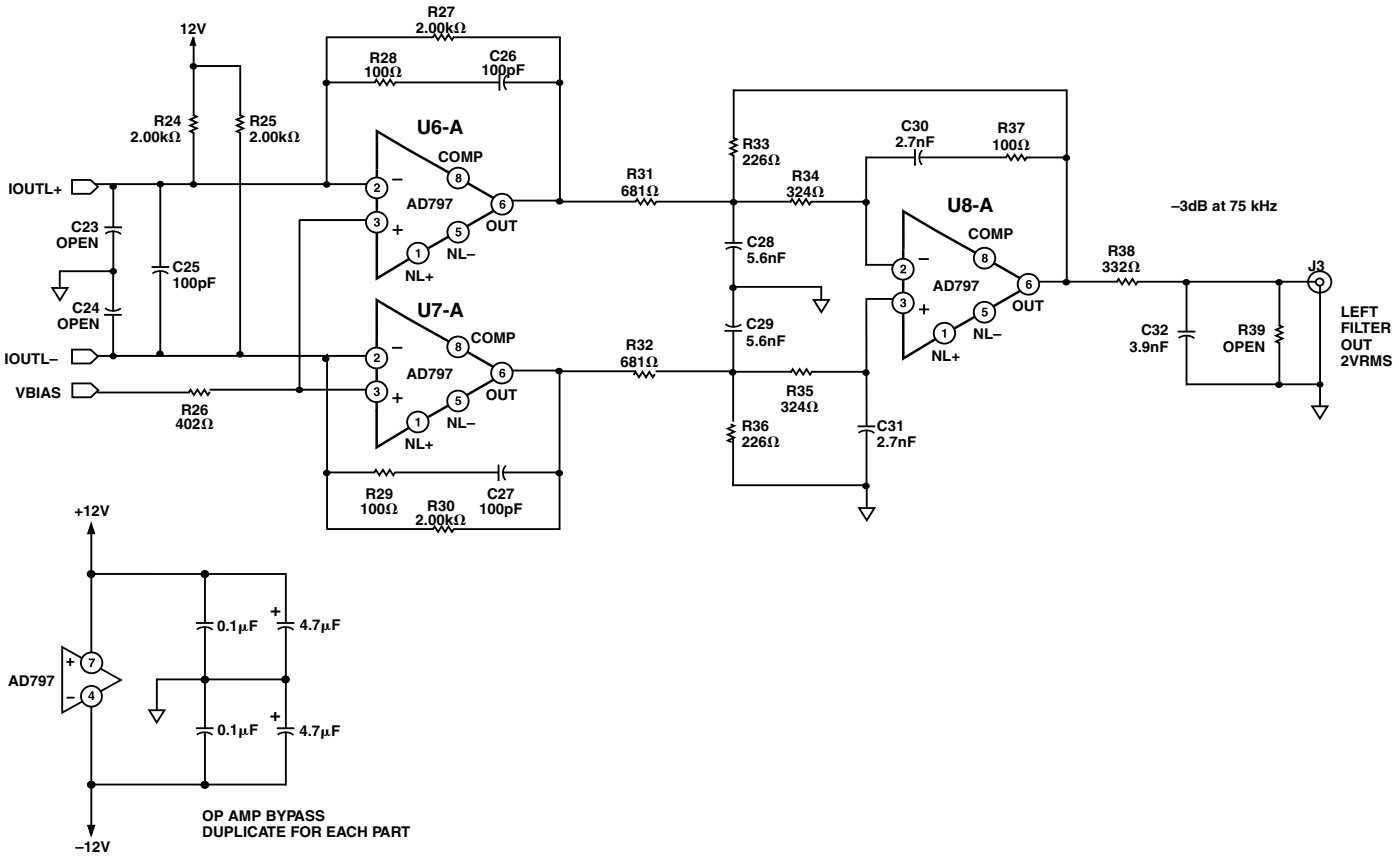


Figure 9. Left Channel Single-Ended Output

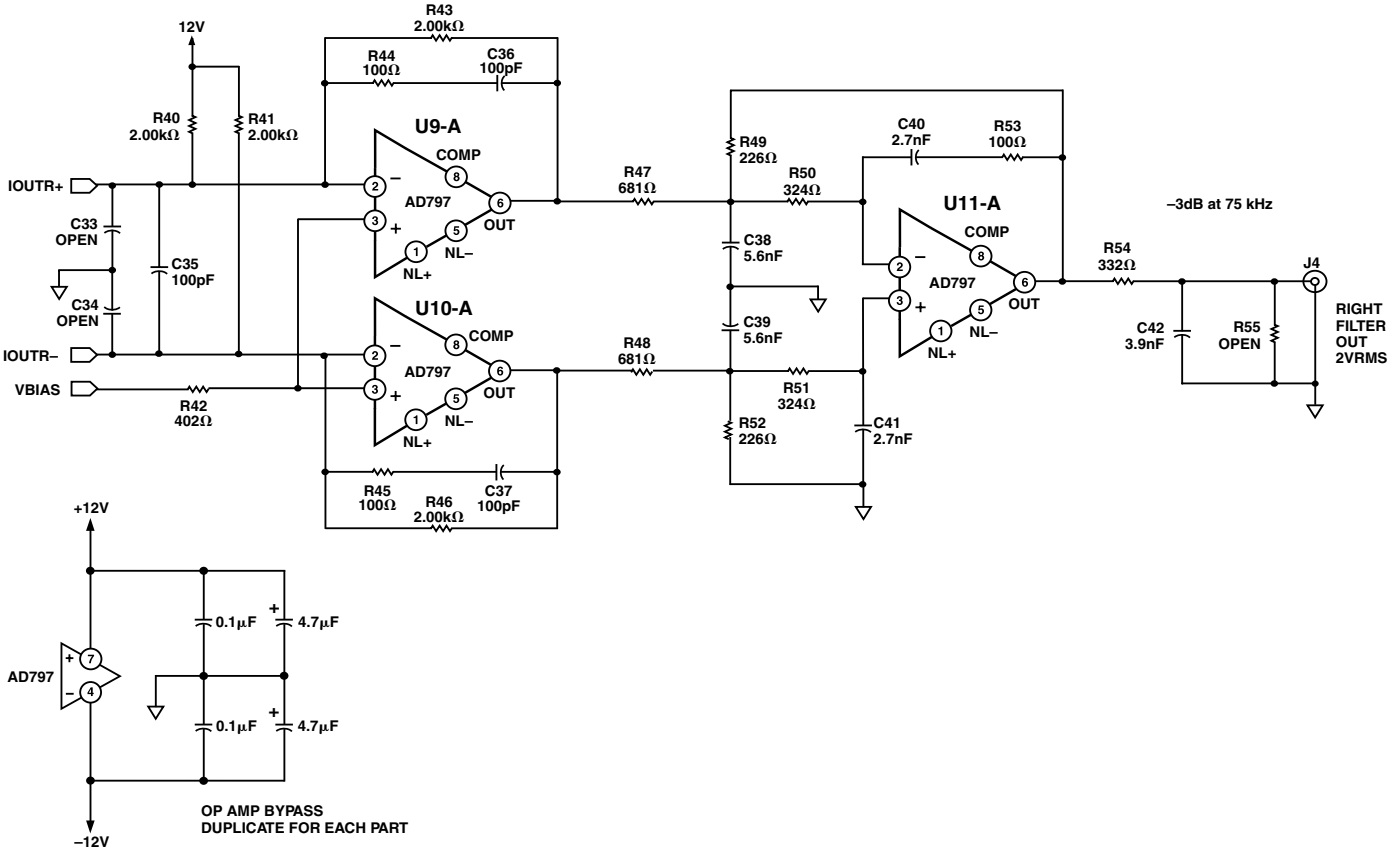


Figure 10. Right Channel Single-Ended Output

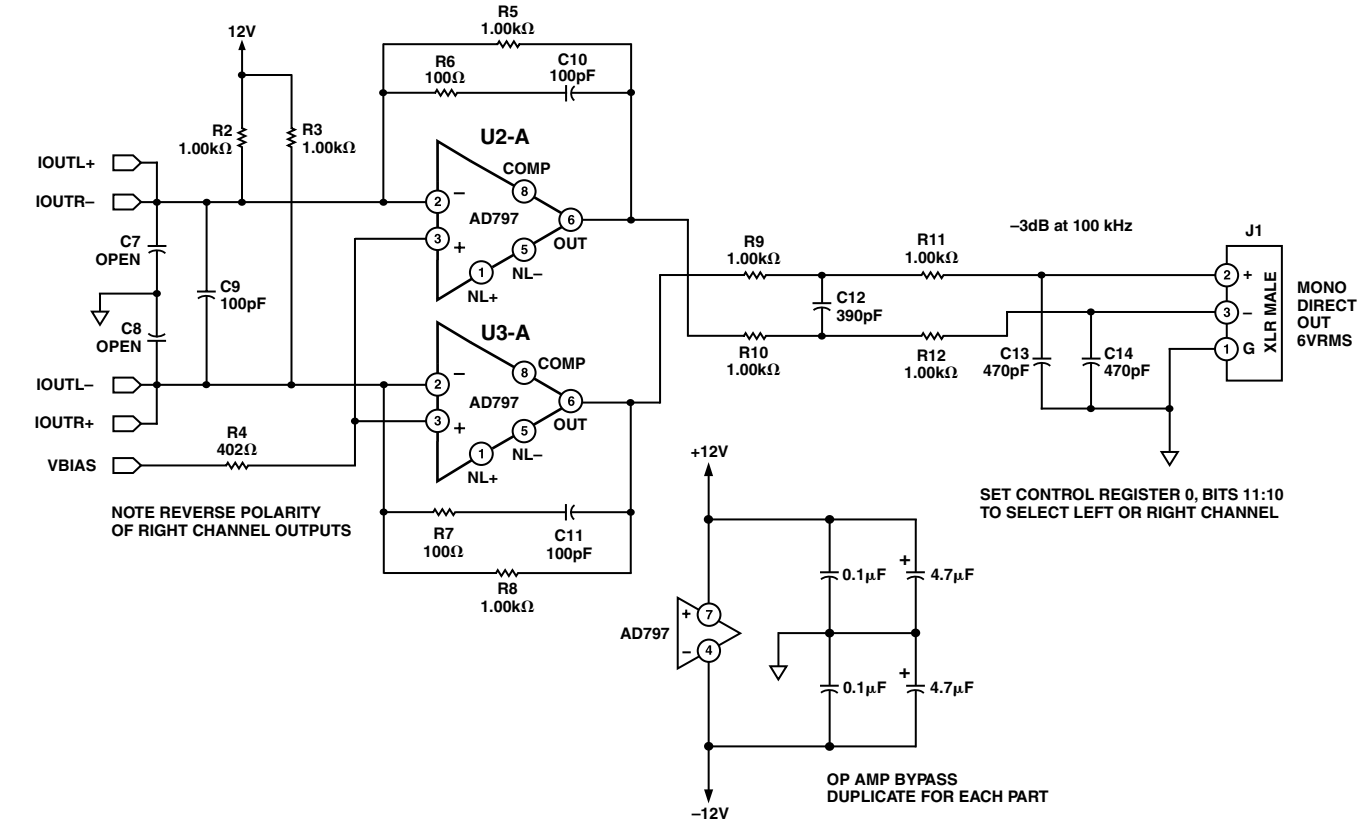


Figure 11. Mono Differential Output

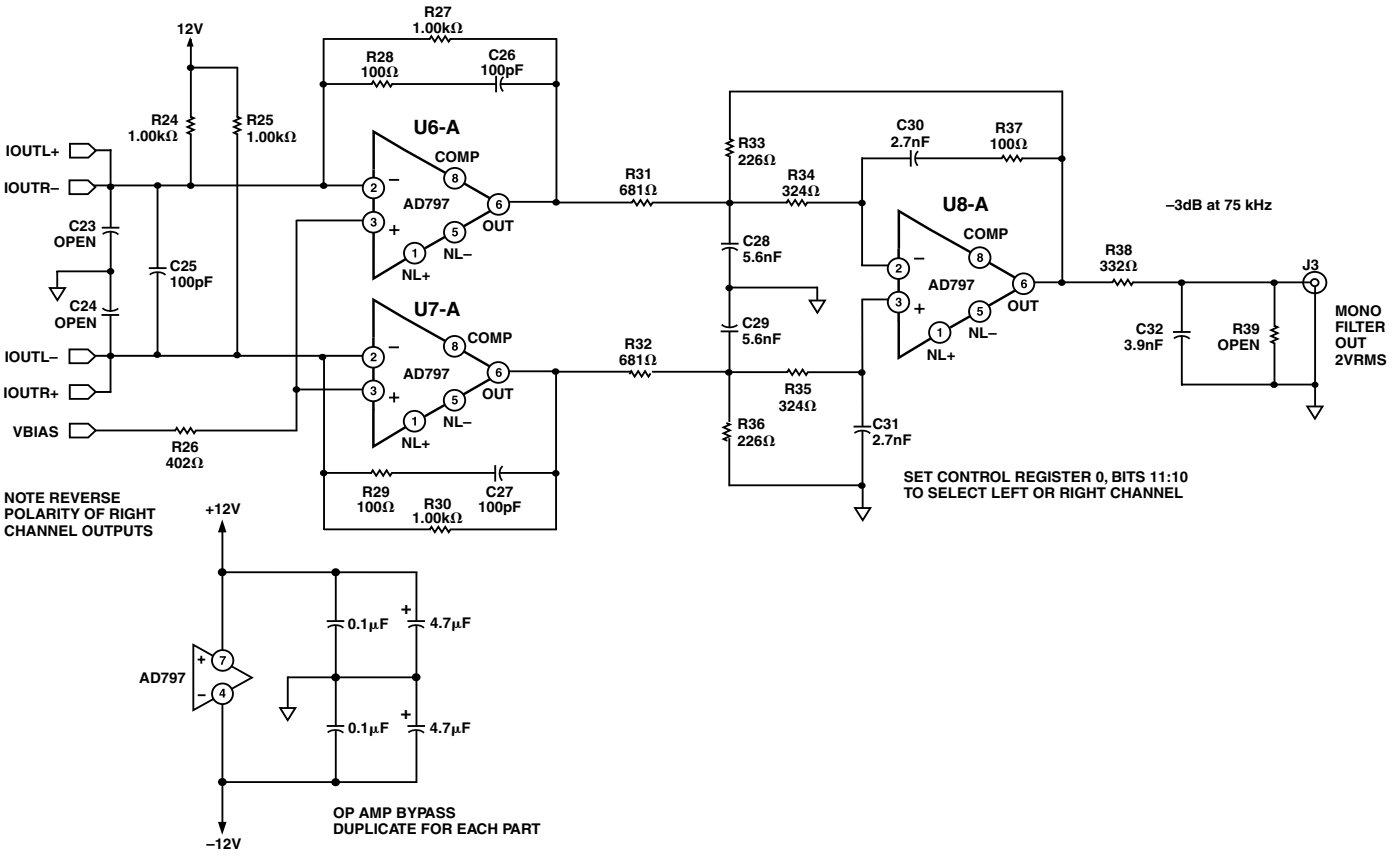
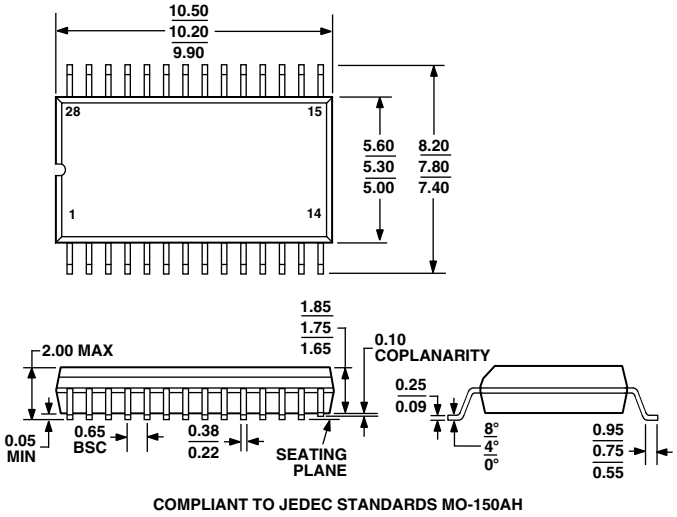


Figure 12. Mono Single-Ended Output

OUTLINE DIMENSIONS

Dimensions shown in millimeters

28-Lead Shrink Small Outline Package (SSOP)
(RS-28)



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